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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,596	12/31/2001	Howard S. David	42390.P13873	2205

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	6

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,596	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed on December 31, 2003 (Paper No. 5).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Saulsbury et al. (US PAT. 6,128,702).

Regarding claim 1, Stracovsky discloses a memory controller, i.e., universal controller (104, figure 1B), comprising an array of tag address storage location, i.e., resource tag (114, figure 1B), and a command sequencer and serializer unit, i.e. command sequencer (116, figure 1B), coupled to the array of tag address storage locations further determent the resources state of and location of the requested data stored in shared memory (108, figure 1B) and (col. 7 line 24 through col. 8 line 2 and col. 10 line 46 through col. 11 line 15), the command sequencer and serializer unit to control a data in a memory module, i.e., shared memory (108, figure 1B) via the

memory command bus (220, figure 1B), command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the memory module (col. 6 lines 21-49, col. 11 line 22 through col. 12 line 19 and col. 13 lines 8-47). Stracovsky differs from the claimed invention in not specifically teaches a data cache located on the memory module and the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module. However, Saulsbury teaches in the computer system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1), in addition, Saulsbury teaches the memory controller is able to accessing the data from the data cache memory via the primary data cache bank logic (150, figure 2) which the memory accessing operation comprising a command to cause a previous line of data, i.e., victim data cache line, to be evicted out of the data cache an eviction buffer, i.e., victim data cache, located on the memory module (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system Stracovsky in having a data cache located on each of memory bank and the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module, as per teaching of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 3, Saulsbury discloses the command sequencer and serializer to deliver a write-back command to the data cache associated with the memory module, the write back

command to cause the previous line of data stored in the eviction buffer to be written out to a memory module memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 4, Saulsbury discloses the write-back command including way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 5, Stracovsky discloses a memory module, i.e., shared memory (108, figure 1B) comprising at least one memory device (device type 1 – device type N, figure 1C), and a memory controller, i.e., universal controller (104, figure 1B) coupled to the shared memory via the memory bus (220, figure 1B), and the memory controller further generating the requested data and command from the processor (102, figure 1B) to the memory device (col. 6 lines 21-49, col. 11 line 22 through col. 12 line 19 and col. 13 lines 8-47), the memory controller including an array of tag address storage location, i.e., resource tag (114, figure 4) and (col. 7 line 24 through col. 8 line 2 and col. 10 line 46 through col. 11 line 15). Stracovsky differs from the claimed invention in not specifically teaches a data cache coupled to the memory device, the memory controller to write a current line of data to the data cache, the memory controller to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory modules. However, Saulsbury a discloses in the computer system (100, figure 1) comprising a memory controller, i.e. CPU (102) and a system memory (103, figure 1) wherein the system memory comprising a plurality of memory block (104, figure), and each memory block comprising data cache bank (122, figure 1) and main memory bank (118, figure 1), in addition, Saulsbury teaches the memory controller is able to accessing the data from the data cache memory via the primary data cache bank logic (150, figure 2) which the memory accessing

operation comprising a command to cause a previous line of data, i.e., victim data cache line, to be evicted out of the data cache an eviction buffer, i.e., victim data cache, located on the memory module (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system Stracovsky in having a data cache located on each of memory bank and the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to an eviction buffer located on the memory module, as per teaching of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 6, Saulsbury discloses the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66).

Regarding claim 7, Saulsbury discloses the memory module to receive a write-back command that generated by the memory controller, the write-back command to cause the previous line of data to be written out of the eviction buffer to the memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 8, Saulsbury discloses the write-back command including way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 9, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller, i.e. universal controller (104, figure 1B) coupled to the processor via the system bus (106, figure 1B), the memory controller including an

array of tag address storage location, i.e., resource tags (114, figure 1B) and a command sequencer and serializer unit, i.e., command sequencer (116, figure 1B) coupled to the array of tag to determent the resources state of and location of the requested data stored in shared memory (108, figure 1B) and (col. 7 line 24 through col. 8 line 2 and col. 10 line 46 through col. 11 line 15), and a memory module (108, figure 1B) coupled to the memory controller via a memory bus (220, figure 1B), the memory module including at least one memory device (device type 1 – device type N, figure 1C). Stracovsky differs from the claimed invention in not specifically teaches a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer. However, Saulsbury teaches such as rejected as the same in claims 1 and 5. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Stracovsky in having a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into an eviction buffer, as per teaching by the computer system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 11, Saulsbury discloses the memory controller to deliver a write-back command to the data cache, the write-back command to cause the previous line to written out of

the eviction buffer to the memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 12, Saulsbury discloses the write-back command including way information and back address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Response to Arguments

4. Applicant's arguments with respect to claims 1, 3-9 and 11-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Zhuo H. Li

March 19, 2004

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100